## 550W, 50V High Power RF LDMOS FETs

### Description

The MK0560VP is a 550-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.6 GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

• Typical performance(on 1.6-30MHz wideband test fixture with device soldered) Signal: pulse CW, pulse width:100us, duty cycle:10%,Vgs=3.25V,Vds=50V,Idq=100mA

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	IDS(A)	Gain(dB)	η(%)
1.6	29	56.8	479	1.63	27.8	62
5	27	56.9	490	1.488	29.9	70
10	26.6	56.7	468	1.436	30.1	70
15	29.6	56.7	468	1.416	27.1	71
20	33.2	56.9	490	1.455	23.7	72
25	33.1	56.7	468	1.449	23.6	69
30	32.8	56.7	468	1.47	23.9	68

Signal: CW Vgs=3.25V,Vds=50V, Idq=100mA

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	IDS(A)	Gain(dB)	η(%)
10	29.7	56.9	490	13.6	27.2	72
20	33.6	56.8	479	13.4	23.2	71
30	34.8	56.8	479	13.7	22	70

### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift

### **Suitable Applications**

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)

- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar



#### Table 1. Maximum Ratings

Rating	Sym	mbol Value				Unit	
DrainSource Voltage	V <sub>DS</sub>	SS			Vdc		
GateSource Voltage	V <sub>GS</sub>	s	-10 to +10			Vdc	
Operating Voltage	VDD	D		+55		Vdc	
Storage Temperature Range	Tst	g	-(	65 to +150		°C	
Case Operating Temperature	Tc			+150		°C	
Operating Junction Temperature	TJ	J		+225		°C	
Table 2. Thermal Characteristics					·		
Characteristic	S	Symbol	Va	alue	U	nit	
Thermal Resistance, Junction to Case		<b>D</b>	-				
T <sub>c</sub> = 85°C, Pout=500W CW,		Rejc	1	BD	ຶ	/W	
Table 3. ESD Protection Characteristics	•				•		
Test Methodology				Class			
Human Body Model (per JESD22A114)				Class 2			
Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)							
Characteristic		Symbol	Min	Тур	Max	Unit	
DC Characteristics			•				
Drain-Source Voltage		N/		400		N	
V <sub>GS</sub> =0, I <sub>DS</sub> =1.0mA		V <sub>(BR)DSS</sub>		122		V	
Zero Gate Voltage Drain Leakage Current							
$(V_{DS} = 50V, V_{GS} = 0 V)$		IDSS			1	μΑ	
Gate—Source Leakage Current					4	٨	
$(V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V})$		I <sub>GSS</sub>			I	μΑ	
Gate Threshold Voltage		M (II)		2.50		V	
$(V_{DS} = 50V, I_D = 600 \ \mu A)$		V <sub>GS</sub> (th)		2.59		V	
Gate Quiescent Voltage		V		2.05		V	
(V <sub>DD</sub> = 50 V, $I_D$ = 100 mA, Measured in Functional Test)		V GS(Q)		5.25		V	
Drain source on state resistance		Pdc(op)		190		mO	
(V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured		Kus(UII)		109		11122	
Common Source Input Capacitance		CISS		158		pF	
$(V_{\text{GS}}$ = 0V, $V_{\text{DS}}$ =50 V, f = 1 MHz) Each section side of device measurements of the transmission of transmission of the transmission of	sured						
Common Source Output Capacitance		Coss		46.8		pF	
$(V_{\text{GS}}$ = 0V, $V_{\text{DS}}$ =50 V, f = 1 MHz) Each section side of device measurements of the transmission of transmission of the transmission of	sured						
Common Source Feedback Capacitance		C <sub>RSS</sub>		1.24		pF	
$(V_{\text{GS}}$ = 0V, $V_{\text{DS}}$ =50 V, f = 1 MHz) Each section side of device measurements $V_{\text{GS}}$ = 0.0 $V_{\text{DS}}$ = 5.0 $V_{\text{S}}$ f = 1 MHz) Each section side of device measurements $V_{\text{GS}}$ = 0.0 $V_{\text{DS}}$ = 0.0 $V$	sured						



Figure 1: 1.6-30MHz wideband test fixture picture



#### BOM of 1.6-30MHz test fixture

C1	1000PF	ATC100B
C2,C8,C9,	2000RE	ATCOOR
C11,C12	3900FF	AICOUD
C3,C13,C14	10UF	10UF/50V
C5,C6	1UF	1UF/50V
C4	100PF	ATC100B
C7,C10	2.2UF	2.2UF/50V
T1	1:04	No 43
T2,T3	17Ω,1000mm	No 73
T4	50Ω,25mm	No 43
L1,L2	18 turns	No 43
R1	51Ω	
R2,R3	1000Ω	

## Package Outline

### Flanged ceramic package; 2 mounting holes; 4 leads





0 5 10 mm L.... scale

UNIT	A	b	с	D	D1	е	E	E1	F	н	H1	L	р	Q	q	U1	U2	W1	W <sub>2</sub>
<b>m</b> m	4.72	3.94	0.15	20.02	19.96	8.89	9.50	9.53	1.14	19.94	12.83	5.33	3.38	1.70	27.04	34.16	9.91	0.25	0.51
	3.43	3.68	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.57	4.32	3.12	1.45	21.34	33.91	9.65	0.20 0.3	0.51
inchos	0.186	0.155	0.006	0.788	0.786	0.35	0.374	0.375	0.045	0.785	0.505	0.210	0.133	0.067	1 100	1.345	0.390	0.01	0.02
Inches	0.135	0.145	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.495	0.170	0.123	0.057	1.100	1.335	0.380	0.01	0.02

OUTLINE		REFERENCE	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC JEITA			
PKG-B4E				$\bigcirc \bigcirc$	03/12/2013

### **Revision history**

#### Table 5. Document revision history

Date	Revision	Datasheet Status
2017/6/27	Rev 1.0	Preliminary Datasheet Creation

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